

IMPLEMENTATION OF FEED FOR WARD NEURAL NETWORK MODULES USING CMOS DESIGN APPROACH

RANITA KHUMUKCHAM, LANTHOI THOKCHOM, B. ATHOI SHARMA, RAJSHREE RAJKUMARI & SOMORJIT SANJENBAM

Department of ECE, Manipur Institute of Technology, Takyelpat, Imphal, India

ABSTRACT

This paper we design an analog circuit implementation, based on a CMOS technology, of the feed forward neural primitives of an on-chip learning architecture implementation approach. Basically our approach is based on current mode computation and is aimed at a low power / low voltage circuit implementation; moreover, it is easily scalable to implement network of any size. TANNER Tool efficient software for the VLSI design is utilized. Schematic of the circuit is designed on S-edit and then its respective output waveform viewed with W-edit. Utilizing Layer edit IC design is fabricated and simulation is successfully done with T-Spice.

KEYWORDS: VLSI, T Spice, CMOS, MLP, TANNER Tool